TSMC-01-1194

March 22, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/754,833 01/09/04

Shu-Ying Cho et al.

TEMPORARY SELF-ALIGNED STOP LAYER IS APPLIED ON SILICON SIDEWALL

INFORMATION DISCLOSURE STATEMENT

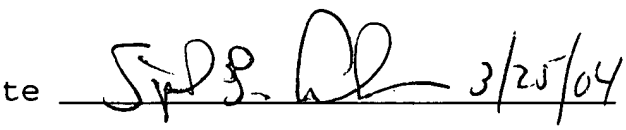
Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 25, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date  3/25/04

U.S. Patent 6,627,502 to Cho, "Method for Forming High Concentration Shallow Junctions for Short Channel MOSFETs," teaches a method for forming shallow LDD diffusions using poly-silicon sidewalls as a diffusion source.

U.S. Patent 6,136,636 to Wu, "Method of Manufacturing Deep Sub-Micron CMOS Transistors," discusses forming nitrogen-doped amorphous silicon layer on the gate structure and on a pad oxide.

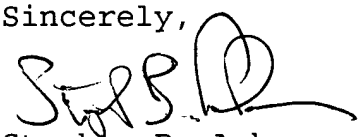
U.S. Patent 5,905,293 to Jeng et al., "LDD Spacers in MOS Devices with Double Spacers," discloses a method of forming an LDD structure with an improved contact etch window and tighter control of LDD length.

U.S. Patent 5,648,287 to Tsai et al., "Method of Salicidation for Deep Quarter Micron LDD MOSFET Devices," discusses a salicide structure which in combination with an LDD structure is used to form quarter micron MOSFETs.

U.S. Patent 6,335,253 to Chong et al., "Method for Form MOS Transistors with Shallow Junctions Using Laser Annealing," describes an alternative method of diffusing a doped impurity.

U.S. Patent 5,391,508 to Matsuoka et al., "Method of Forming Semiconductor Transistor Devices," discusses an example of shallow source/drain regions. Thermal diffusion from a semiconductor sidewall on the gate electrode drives implanted ions into the substrate to form shallow source/drain regions.

Sincerely,



Stephen B. Ackerman,
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Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-01-1194	10/754,833
Applicant: Shu-Ying Cho et al.	
Filing Date: 01/09/04	Group Art Unit:

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6627502	9/30/03	Cho	438	265	10/24/02
	6136636	10/24/00	Wu	438	231	4/14/99
	5905293	5/18/99	Jeng et al.	257	408	4/6/98
	5648287	7/15/97	Tsai et al.	437	44	10/11/96
	6335253	1/1/02	Chong et al.	438	305	7/12/00
	5391508	2/21/95	Matsuoka et al.	437	41	12/21/93

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.